Intel® Desktop Board D845HV Specification Update

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The Intel® Desktop Board D845HV may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
September 2001	-001	This document is the first Specification Update for the Intel® Desktop Board D845HV.
October 2001	-002	Added Erratum 1.
November 2001	-003	Updated Erratum 1.
December 2001	-004	Added Specification Change 1.
January 2002	-005	Updated General Information section. Added Erratum 2. Added Specification Clarifications 1, 2.
February 2002	-006	Added Erratum 3. Updated General Information.

PREFACE

This document is an update to the specifications contained in the *Intel® Desktop Board D845HV Technical Product Specification* (Order number A65136). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order number 249199) for specification updates concerning the Intel Pentium 4 processor. Items contained in the *Intel Pentium 4 Processor Specification Update* that either do not apply to the desktop board D845HV or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel®* 82845 *Chipset:* 82845 *Memory Controller Hub (MCH) Specification Update* (Order Number 290659) for specification updates concerning the 82845 MCH Controller. Items contained in the 82845 *MCH Specification Update* that either do not apply to the desktop board D845HV or have been worked around are noted in this document. Otherwise, it should be assumed that any MCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82801 I/O Controller Hub (ICH) Specification Update* (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the *Intel 82801 ICH Specification Update* that either do not apply to the desktop board D845HV or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *Intel® 82802 Firmware Hub (FWH) Specification Update* (Order Number TBD) for specification updates concerning the 82802 Firmware Hub. Items contained in the *Intel 82802 FWH Specification Update* that either do not apply to the desktop board D845HV or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D845HV's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for the Intel® Desktop Board D845HV

GENERAL INFORMATION

Basic Desktop Board D845HV Identification Information

AA Revision	PBA Revision	BIOS Revision	Notes
A68838-304	A68837-304	HV84510A.86A.0018.P04	1-6
A68838-306	A68837-306	HV84510A.86A.0022.P05	1-6
A68838-307	A68837-307	HV84510A.86A.0029.P07	1-6
A68840-305	A68839-305	HV84510A.86A.0018.P04	1-6
A68840-307	A68839-307	HV84510A.86A.0022.P05	1-6
A68840-308	A68839-308	HV84510A.86A.0029.P07	1-6
A63927-304	A63926-304	HV84510A.86A.0018.P04	1-6
A63927-305	A63926-305	HV84510A.86A.0022.P05	1-6
A63927-306	A63926-306	HV84510A.86A.0029.P07	1-6
A63929-305	A63928-305	HV84510A.86A.0018.P04	1-6
A63929-306	A63928-306	HV84510A.86A.0022.P05	1-6
A63929-307	A63928-307	HV84510A.86A.0029.P07	1-6
A69283-301	A69281-301	HV84510A.86A.0018.P04	1-6
A69283-302	A69281-302	HV84510A.86A.0018.P04	1-6
A69283-303	A69281-303	HV84510A.86A.0029.P07	1-6
A70828-303	A70827-303	HV84510A.86A.0022.P05	1-6
A70828-304	A70827-304	HV84510A.86A.0022.P05	1-6
A70828-305	A70827-305	HV84510A.86A.0029.P07	1-6

NOTES:

1. The PBA number or AA number is found on a small label on the component side of the board.
2. The 82845 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
RG82845 MCH	A3	SL5V7
82801BA ICH	C0	SL5PN
N82802AB 4Mbit FWH	A1	SB48

3. The following errata are contained in the *Intel® Pentium® 4 Processor Specification Update* (Order Number 249199) for the Pentium 4 processor and either do not apply to the desktop board D845HV or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
4. The following items are contained in the *Intel® 82845 Memory Controller Hub (MCH) Specification Update* (Order Number 290659) and either do not apply to the desktop board D845HV or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the MCH apply to this PBA revision.
5. The following items are contained in the *Intel® 82801 I/O Controller Hub Specification Update* (Order Number 290677) and either do not apply to the desktop board D845HV or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.
6. The following items are contained in the *Intel® 82802 Firmware Hub Specification Update* (Order Number TBD) and either do not apply to the desktop board D845HV or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the FWH apply to this PBA revision.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the desktop board D845HV. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the desktop board, driver, or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Change to description of Section 1.6, Processors
NO.	**PLANS**	**ERRATA**
1	Fixed	Certain PCI Add-in devices may not be recognized
2	Fixed	A system hang during POST may occur when using a Pentium® 4 processor at a speed of 1.6 GHz in conjunction with a single SDRAM DIMM configuration.
3	Fix	System hang during POST may occur when using certain USB cameras
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Change to description of Section 2.6, Interrupts
2	Doc	Change to description of Section 2.7, PCI Interrupt Routing Map

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Desktop Board D845HV Technical Product Specification* (Order Number A65136). All Specification Changes will be incorporated into a future version of that specification.

1. Change to Description of Section 1.6, Processors

Section 1.6, Processors, removes support for the 1.4 GHz Pentium® 4 processor and will change in its entirety as follows:

1.6 Processor

CAUTION

Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D845HV/D845WN Specification Update *for the most up-to-date list of supported processors for these boards.*

The D845HV and D845WN boards support a single Pentium 4 processor (in an mPGA478 socket) with a system bus of 400 MHz. The D845HV and D845WN boards support the processors listed in Table 5. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	1.5, 1.6, 1.7, 1.8, 1.9, and 2.0 GHz	400 MHz	256 KB

NOTE

Use only ATX12V- or SFX12V-compliant power supplies with the D845HV and D845WN boards. ATX12V and SFX12V power supplies have an additional power lead that provides required supplemental power for the Intel® Pentium 4 processor. Always connect the 20-pin and 4-pin leads of ATX12V and SFX12V power supplies to the corresponding connectors on the D845HV and D845WN boards, otherwise the board will not boot.

Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

For information about	Refer to
Processor support	Section 1.3, page 17
Processor usage	Section 1.3, page 17
Power supply connectors	Section 2.8.2.3, page 58

ERRATA

1. Certain PCI Add-in Devices May Not be Recognized

PROBLEM: Some add-in PCI devices, especially those that use serial EPROM's, may not be enumerated during POST.

IMPLICATION: Enumeration of certain add-in PCI devices may not occur, particularly if those devices utilize a serial EPROM.

WORKAROUND: For those devices exhibiting this erratum, place the device into PCI slot one (slot one being the slot closest to the processor).

STATUS: This erratum was fixed in BIOS revision HV84510A.86A.0022.P05.

2. A System Hang During POST May Occur When Using a Pentium® 4 Processor at a Speed of 1.6 GHz in Conjunction With a Single SDRAM DIMM Configuration.

PROBLEM: While booting the system, some boards may experience a hang during POST code D3 when the system is configured specifically with a Pentium® 4 processor running at a speed of 1.6 GHz and with only a single SDRAM DIMM installed.

IMPLICATION: There are two failing results to this specific configuration. One is due to false tasks on the SMBus that halts the system during Non-SPD memory detection. The other is due to a violation of specifications in memory initialization. After memory is initialized there exists a requirement that no reads happen for the next 200 µsec, this requirement is violated in the original reference code located in the BIOS.

WORKAROUND: Either add a different speed Pentium 4 processor and/or add additional SDRAM DIMM's to the configuration.

STATUS: This erratum was fixed in BIOS revision HV84510A.86A.0029.P07.

3. System Hang During POST May Occur When Using Certain USB Cameras

PROBLEM: During the system boot, certain USB cameras may cause a hang during POST if the camera is on during the boot process.

IMPLICATION: Some USB cameras may cause a system hang if the camera is on during system boot due to the BIOS incorrectly identifying the camera as a bootable device.

WORKAROUND: Ensure that the USB camera is off during the system boot process.

STATUS: This erratum may be fixed in a future BIOS revision.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Desktop Board D845HV Technical Product Specification* (Order Number A65136). All Specification Clarifications will be incorporated into a future version of that specification.

1. Change to Description of Section 2.6, Interrupts

Section 2.6, Interrupts, will change in its entirety as follows:

2.6 Interrupts

The Interrupts can go through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the Intel ICH2 component. The PIC is supported in Windows* 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and support a total of 24 interrupts.

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for Intel ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16	AGP video (through PIRQA) (Note 2)

continued

Table 16. Interrupts (continued)

IRQ	System Resource
17	AC' 97 Audio/User Available (through PIRQB) (Note 2)
18	User available (through PIRQC) (Note 2)
19	Intel® ICH2 USB Controller #1 (through PIRQD) (Note 2)
20	Intel ICH2 LAN (optional) (through PIRQE) (Note 2)
21	User available (through PIRQF) (Note 2)
22	User available (through PIRQG) (Note 2)
23	Intel ICH2 USB Controller #2/ User Available (through PIRQH) (Note 2)

Note 1: Default, but can be changed to another IRQ.

Note 2: Available in APIC mode only.

2. Change to Description of Section 2.7, PCI Interrupt Routing Map

Section 2.7, PCI Interrupt Routing Map, will change in its entirety as follows:

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The Intel ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D845HV and D845WN boards and therefore share the same interrupt. Table 17 shows an example of how the PIRQ signals are routed on the D845HV and D845WN boards.

For example, using Table 17 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 4 now shares interrupts with these onboard interrupt sources.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	Intel ICH2 PIRQ Signal Name				
	PIRQF	**PIRQG**	**PIRQH**	**PIRQB**	**Other**
AGP connector				INTB	INTA to PIRQA
Intel® ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
Intel ICH2 USB controller #2			INTC		
Intel ICH2 Audio / Modem				INTB	
Intel ICH2 LAN					INTA to PIRQE
PCI Bus Connector 1	INTA	INTB	INTC	INTD	
PCI Bus Connector 2	INTD	INTA	INTB	INTC	
PCI Bus Connector 3	INTC	INTD	INTA	INTB	
PCI Bus Connector 4 (Note)	INTB	INTC	INTD	INTA	
PCI Bus Connector 5 (Note)	INTA	INTB	INTC	INTD	
PCI Bus Connector 6 (Note)	INTB	INTC	INTD	INTA	

Note: D845WN board only.

NOTE

In PIC mode, the Intel ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12,14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In APIC mode, the allocation of PIRQ lines to IRQ signals is as shown in Table 17.